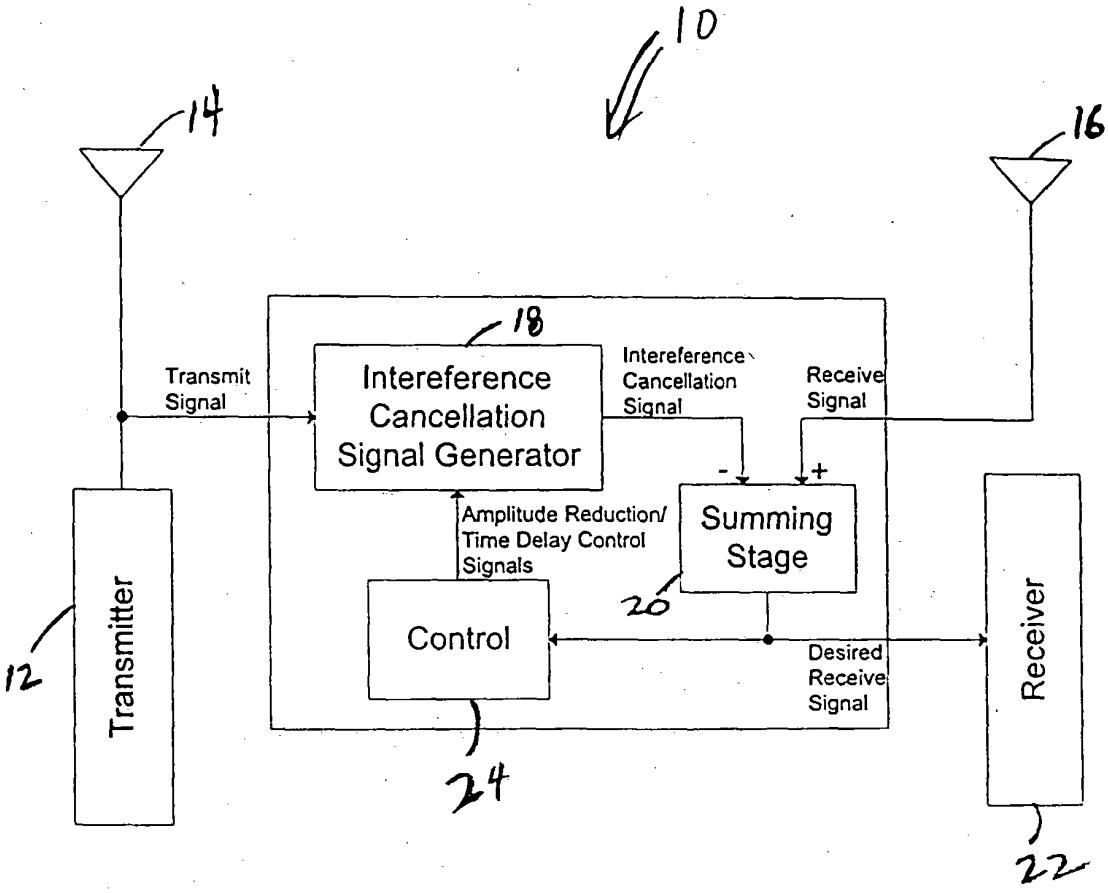

10
14
16
18
Transmit Signal
Intereference Cancellation Signal Generator
Intereference Cancellation Signal
Receive Signal
-
+
Amplitude Reduction/ Time Delay Control Signals
Summing Stage
20
Control
Transmitter
12
Receiver
Desired Receive Signal
24
22

FIG. 1

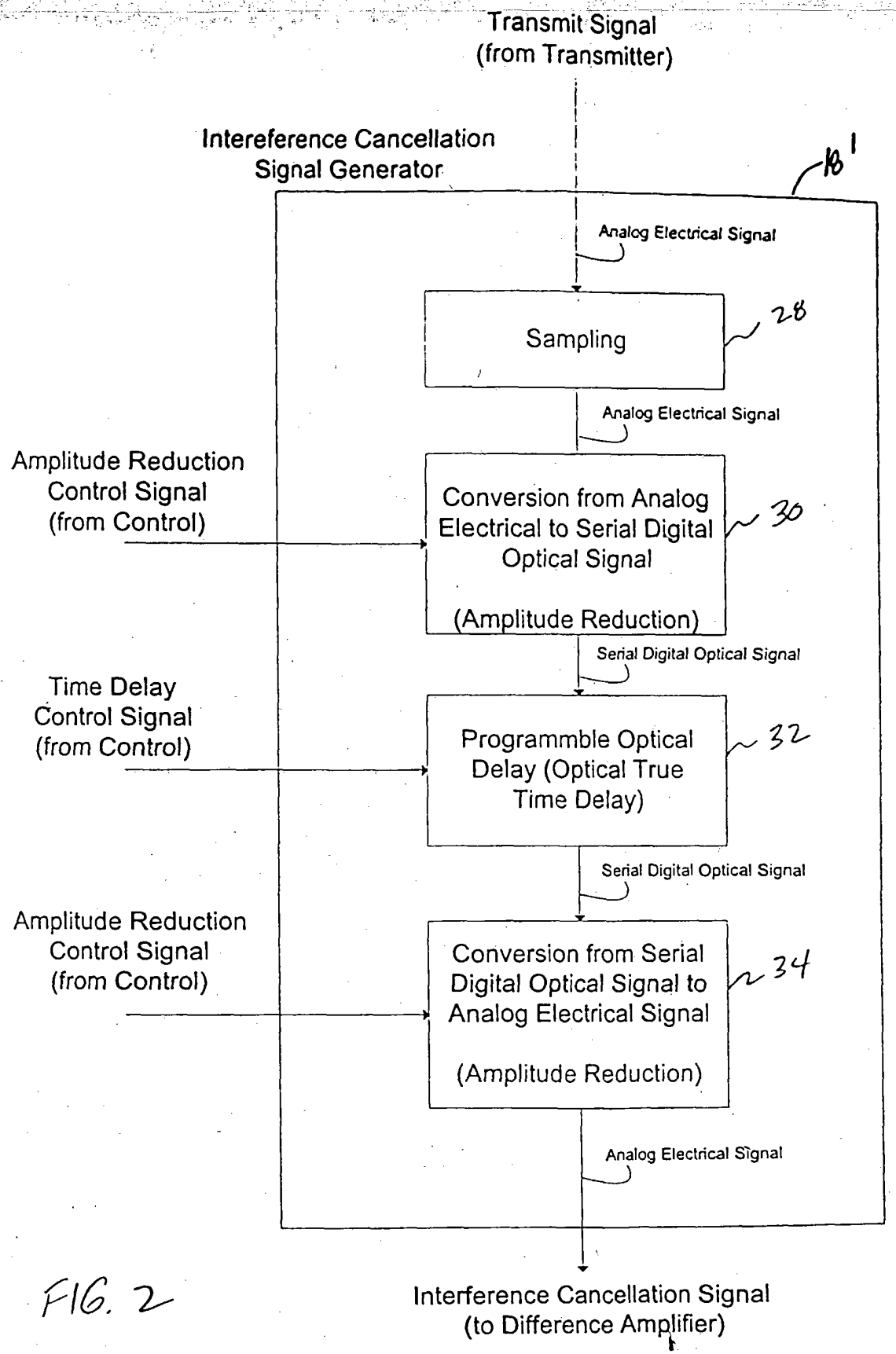

Transmit Signal
(from Transmitter)
Intereference Cancellation
Signal Generator
18'
Analog Electrical Signal
Sampling
28
Analog Electrical Signal
Amplitude Reduction
Control Signal
(from Control)
Conversion from Analog
Electrical to Serial Digital
Optical Signal
(Amplitude Reduction)
30
Serial Digital Optical Signal
Time Delay
Control Signal
(from Control)
Programmble Optical
Delay (Optical True
Time Delay)
32
Serial Digital Optical Signal
Amplitude Reduction
Control Signal
(from Control)
Conversion from Serial
Digital Optical Signal to
Analog Electrical Signal
(Amplitude Reduction)
34
Analog Electrical Signal
Interference Cancellation Signal
(to Difference Amplifier)

FIG. 2

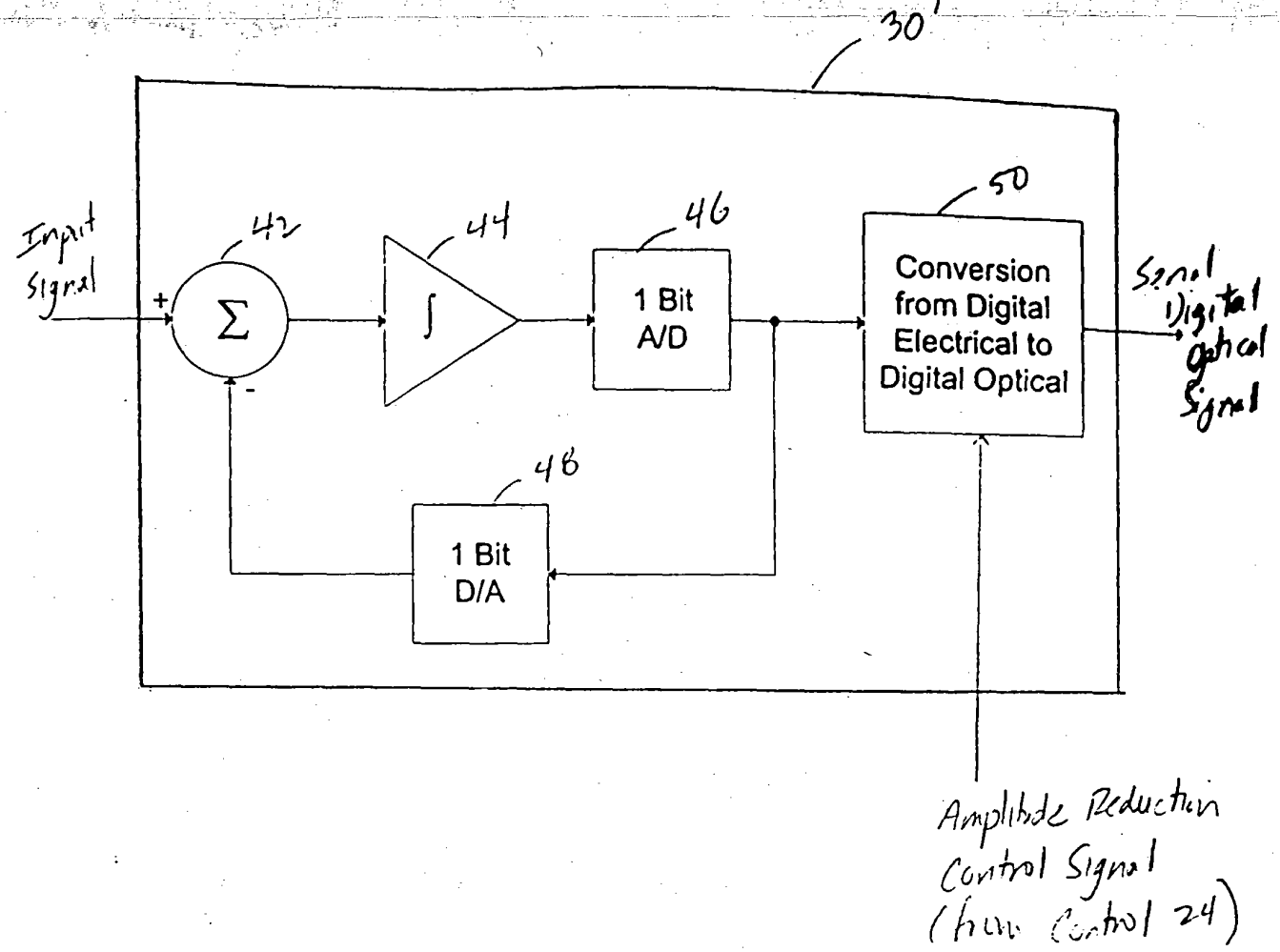

30'
Input Signal
42
44
46
50
+
-
Σ
∫
1 Bit A/D
Conversion from Digital Electrical to Digital Optical
Signal Digital Optical Signal
48
1 Bit D/A
Amplitude Reduction Control Signal (from Control 24)

FIG. 3A

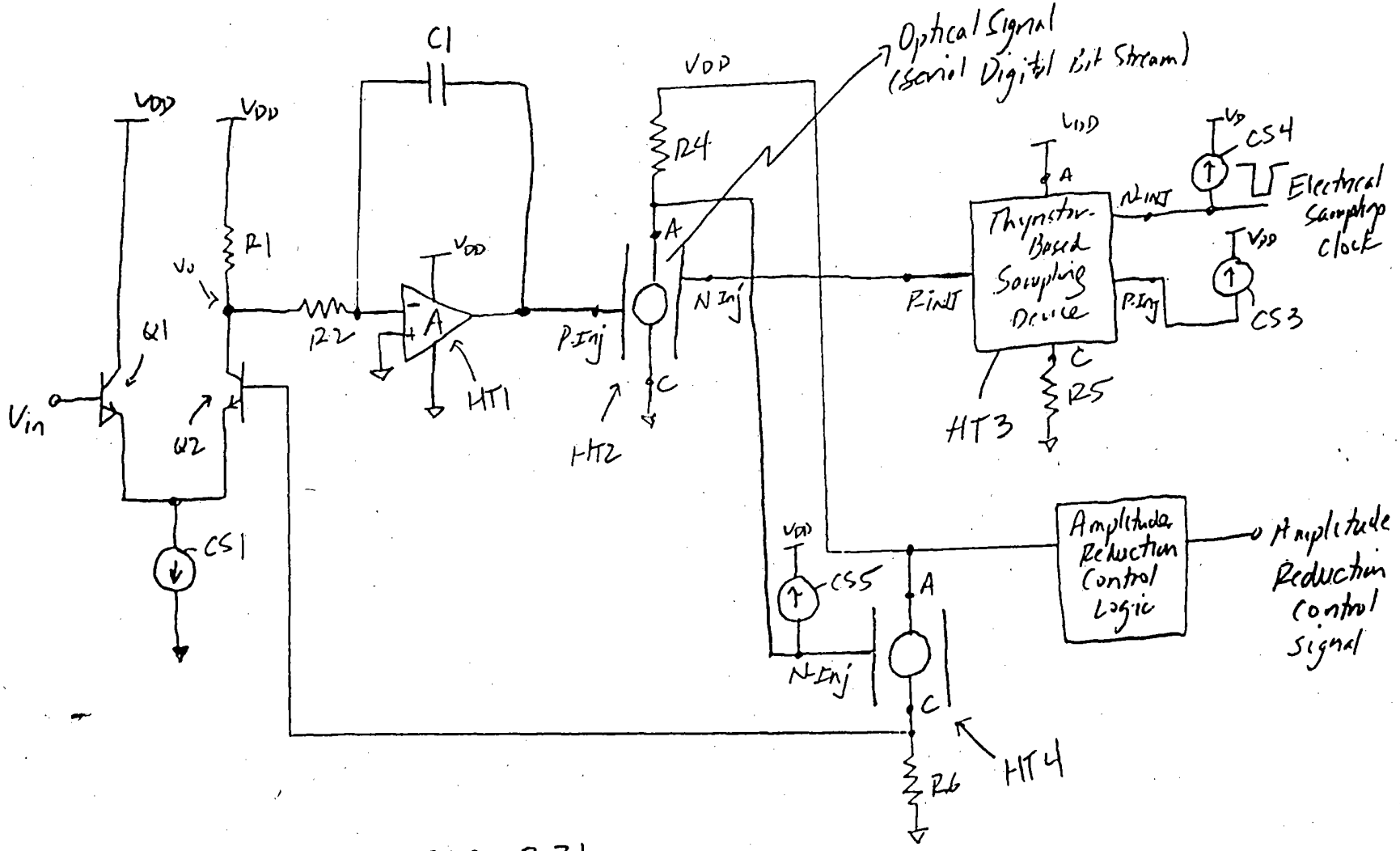

C1
VDD
Optical Signal
(Serial Digital Bit Stream)
R4
A
N Inj
P Inj
C
HT2
HT1
R1
R2
Vo
Q1
Q2
Vin
CS1
Thyristor-Based Sampling Device
P INJ
N INJ
HT3
R5
CS4
Electrical sampling clock
CS3
CS5
Amplitude Reduction Control Logic
Amplitude Reduction control signal
R6
HT4

FIG. 3B1

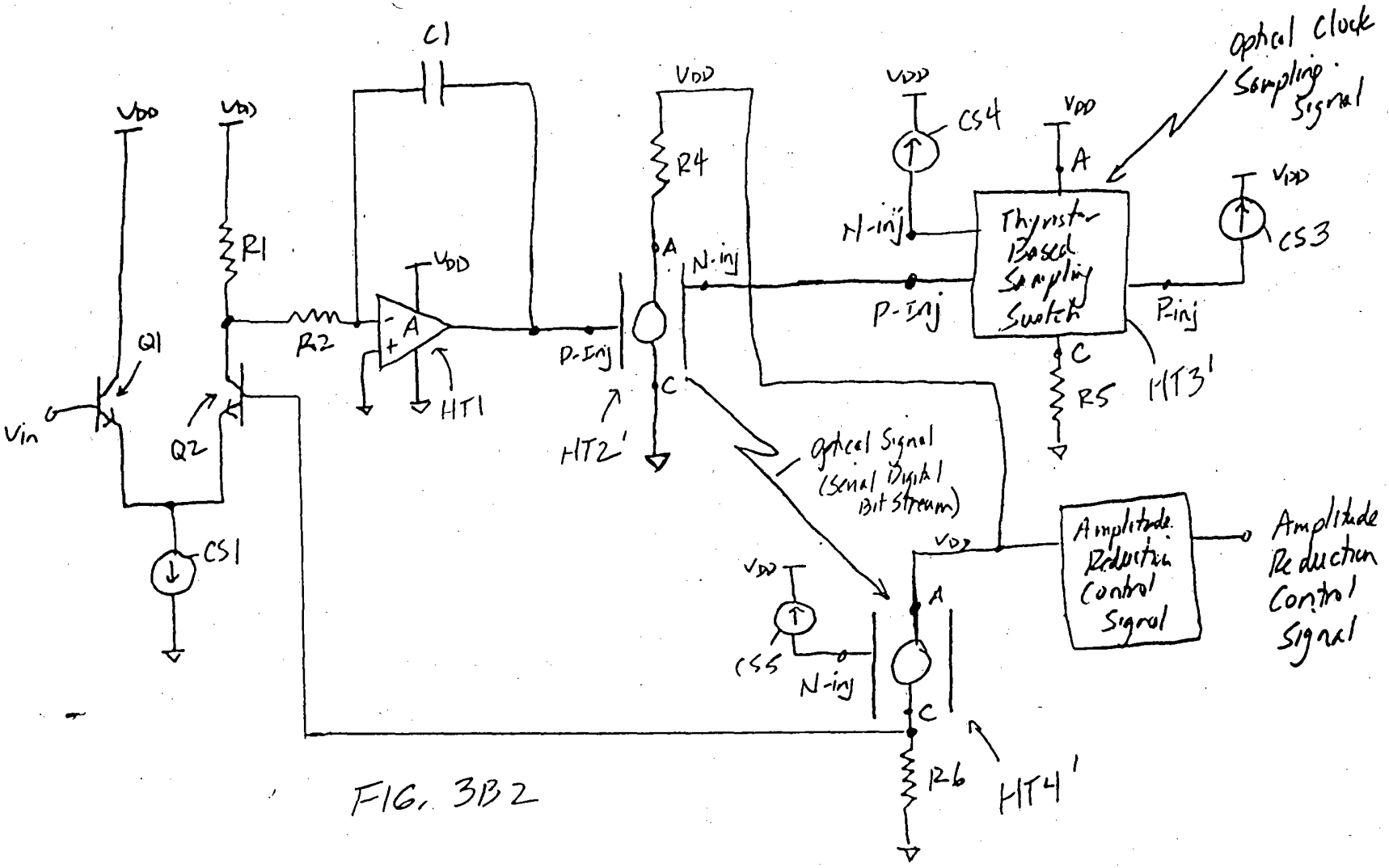

C1
VDD
VDD
VDD
VDD
VDD
R1
R2
R4
R5
R6
Q1
Q2
Vin
CS1
CS3
CS4
CS5
HT1
HT2'
HT3'
HT4'
P-Inj
N-inj
A
C
Optical Clock Sampling Signal
Thyristor Based Sampling Switch
Optical Signal (Serial Digital Bit Stream)
Amplitude Reduction Control Signal
Amplitude Reduction Control Signal

FIG. 3B2

FIG. 3C1

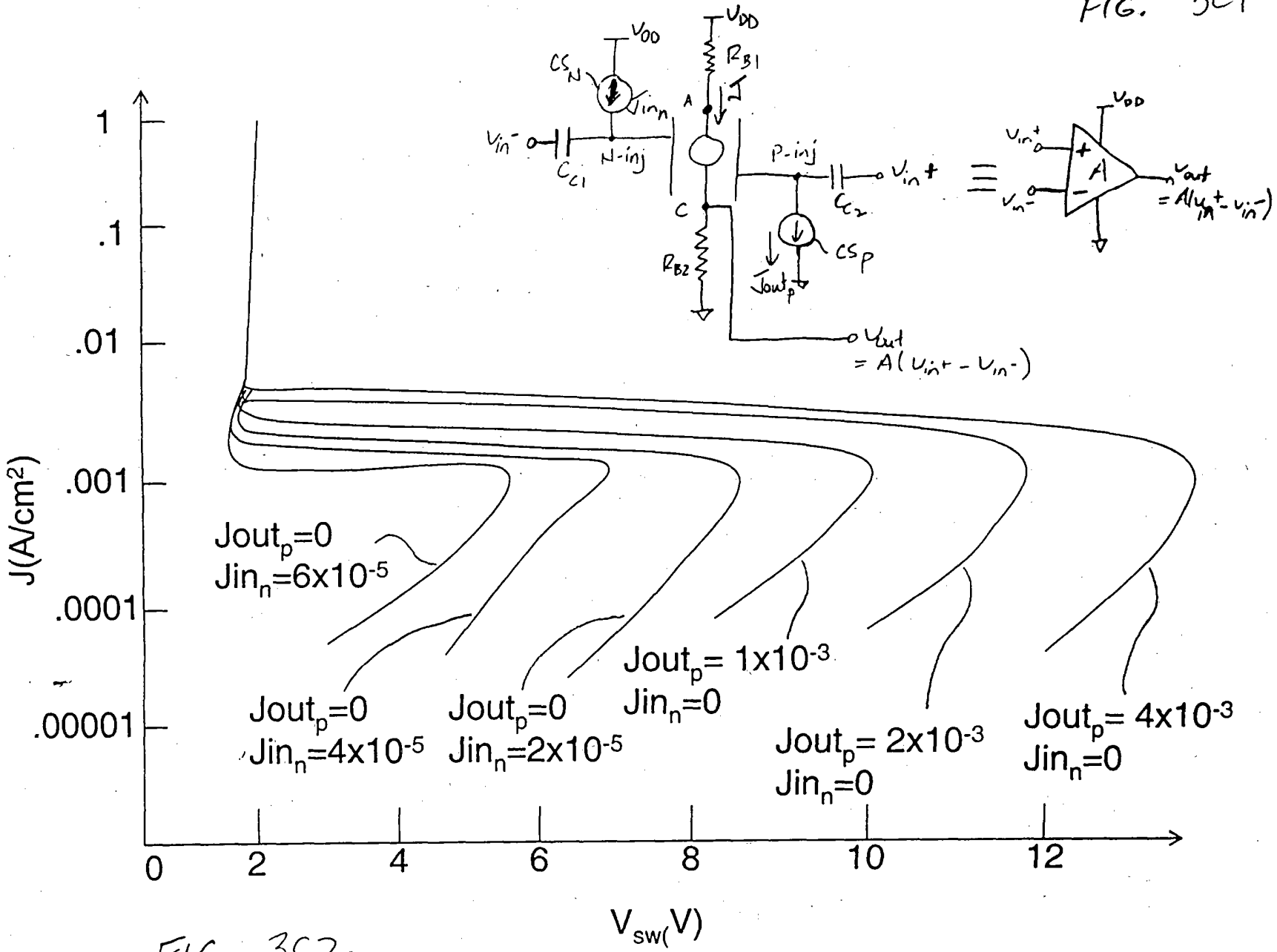


FIG. 3C2

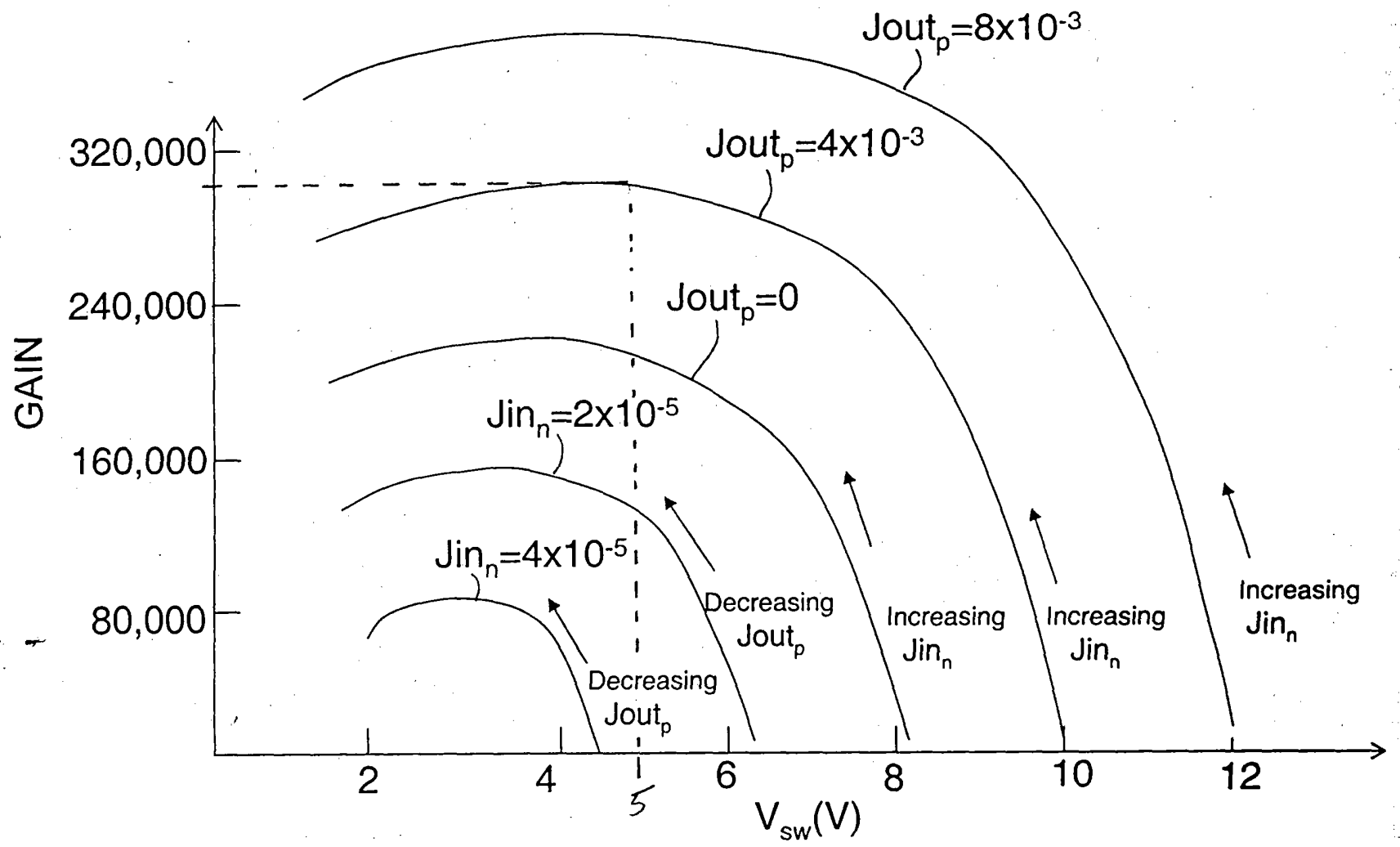

Jout$_p$=8x10^{-3}
Jout$_p$=4x10^{-3}
Jout$_p$=0
Jin$_n$=2x10^{-5}
Jin$_n$=4x10^{-5}
GAIN
320,000
240,000
160,000
80,000
Decreasing Jout$_p$
Decreasing Jout$_p$
Increasing Jin$_n$
Increasing Jin$_n$
Increasing Jin$_n$
2
4
5
6
8
10
12
V$_{sw}$(V)

FIG. 3C3

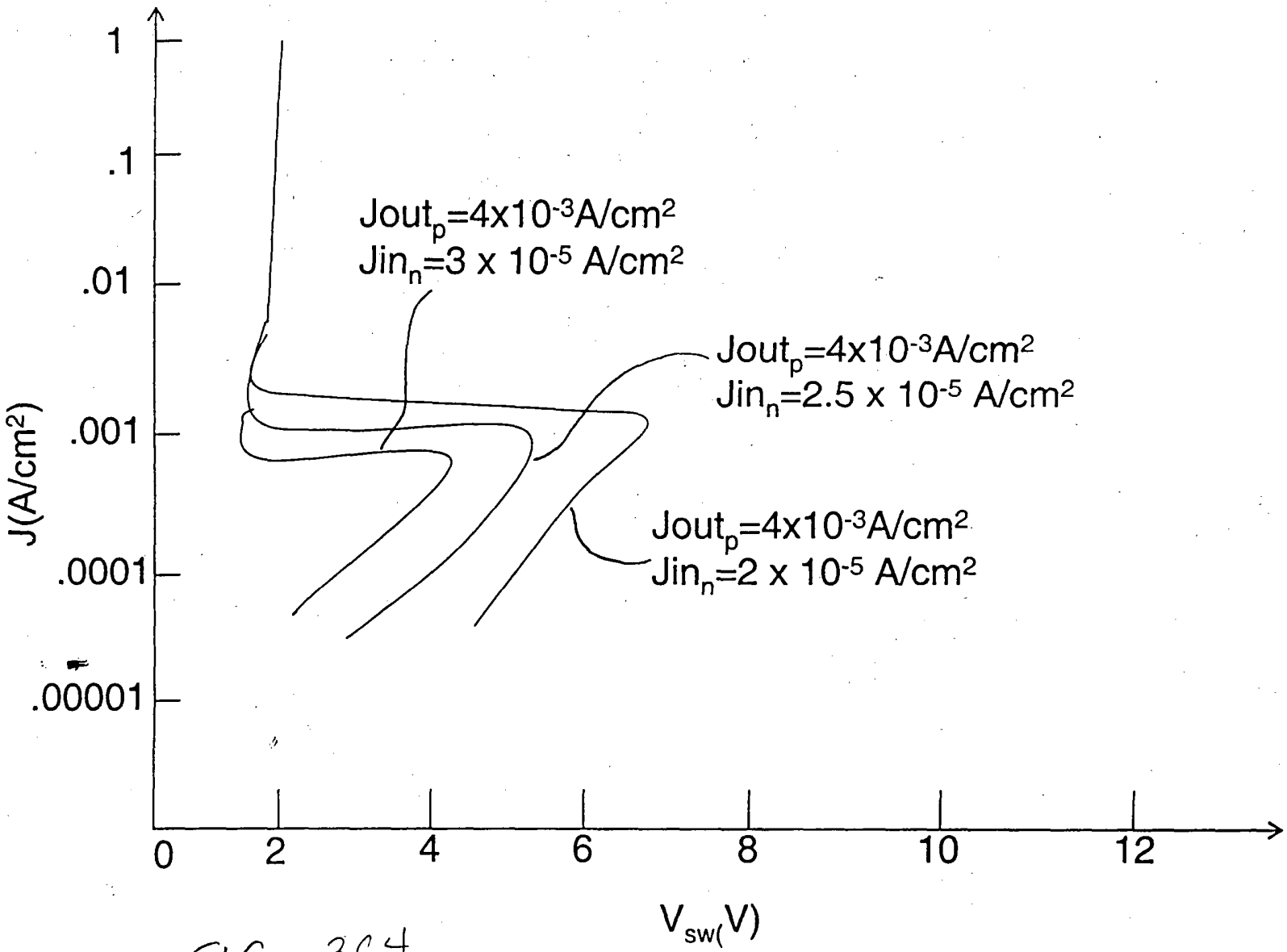

1
.1
.01
.001
.0001
.00001
J(A/cm²)
Jout$_p$=4x10^{-3}A/cm²
Jin$_n$=3 x 10^{-5} A/cm²
Jout$_p$=4x10^{-3}A/cm²
Jin$_n$=2.5 x 10^{-5} A/cm²
Jout$_p$=4x10^{-3}A/cm²
Jin$_n$=2 x 10^{-5} A/cm²
0
2
4
6
8
10
12
V$_{sw}$(V)

FIG. 3C4

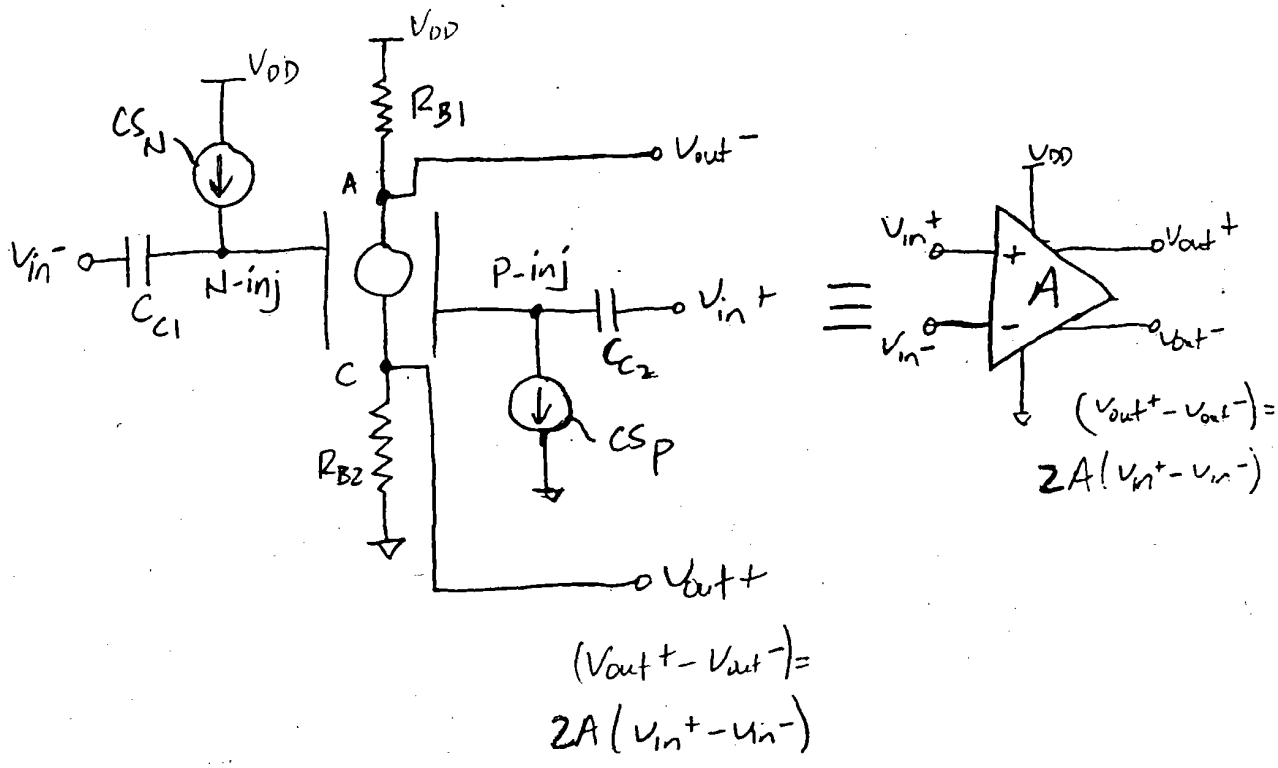

V_{DD}
V_{DD}
CS_N
R_{B1}
A
$V_{out}-$
$V_{in}-$
N-inj
C_{C1}
P-inj
$V_{in}+$
C_{C2}
C
CS_P
R_{B2}
$V_{out}+$
$(V_{out}+ - V_{out}-) =$
$2A(V_{in}+ - V_{in}-)$
$\equiv$
V_{DD}
$V_{in}+$
$V_{out}+$
+
A
-
$V_{in}-$
$V_{out}-$
$(V_{out}+ - V_{out}-) =$
$2A(V_{in}+ - V_{in}-)$

FIG. 3C5

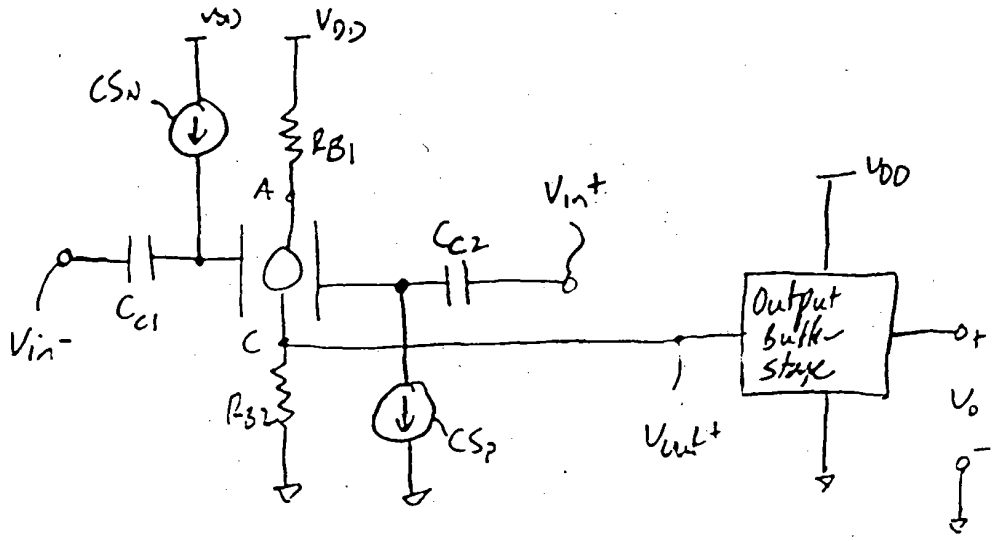
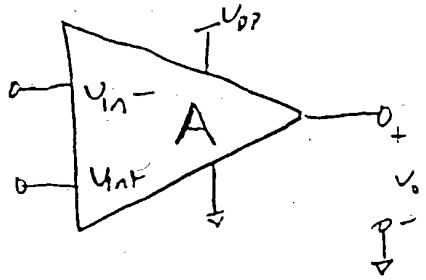


FIG. 3C6 where $V_o \approx -A(V_{in+} - V_{in-})$



where $V_o \approx -A(V_{in+} - V_{in-})$

FIG. 3C7

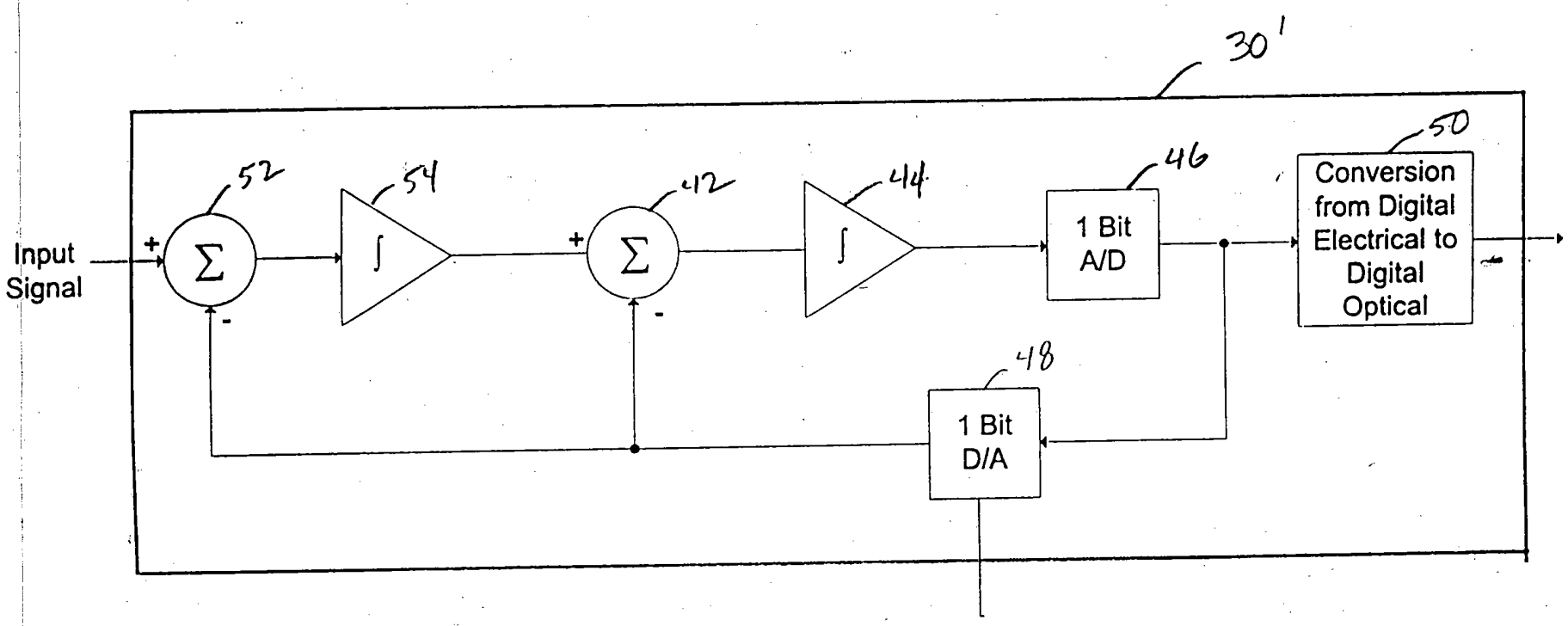

30'
52
54
42
44
46
50
Input Signal
+
Σ
-
∫
+
Σ
-
∫
1 Bit A/D
Conversion from Digital Electrical to Digital Optical
48
1 Bit D/A
Amplitude Reduction Control Signal

FIG. 4A

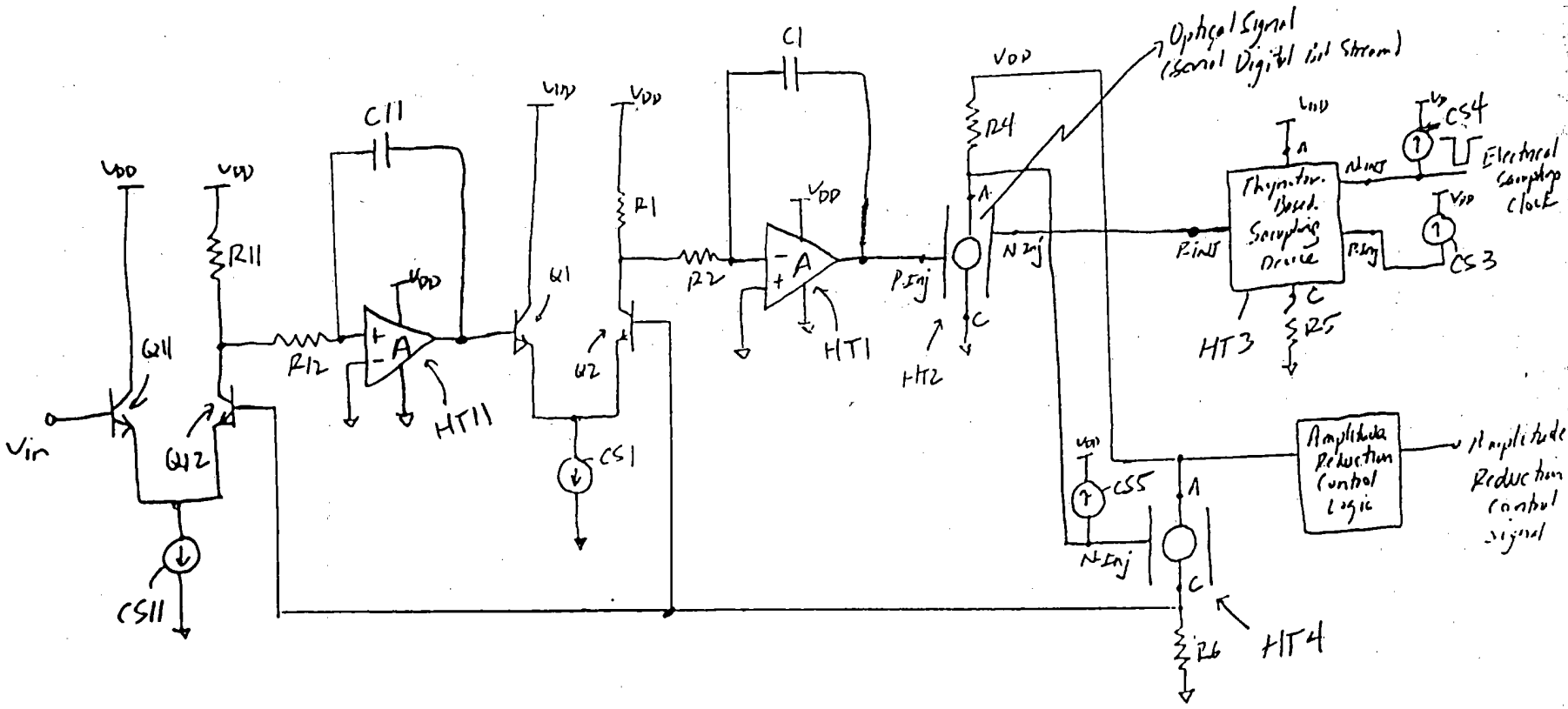

Optical Signal (Serial Digital bit Stream)
Electrical sampling clock
Amplitude Reduction control signal
Thyristor Based Sampling Device
Amplitude Reduction Control Logic
C1
C11
R1
R11
R12
R2
R4
R5
R6
Q1
Q2
Q11
Q12
HT1
HT11
HT2
HT3
HT4
CS1
CS11
CS3
CS4
CS5
PInj
NInj
Vin
VDD

FIG. 4B1

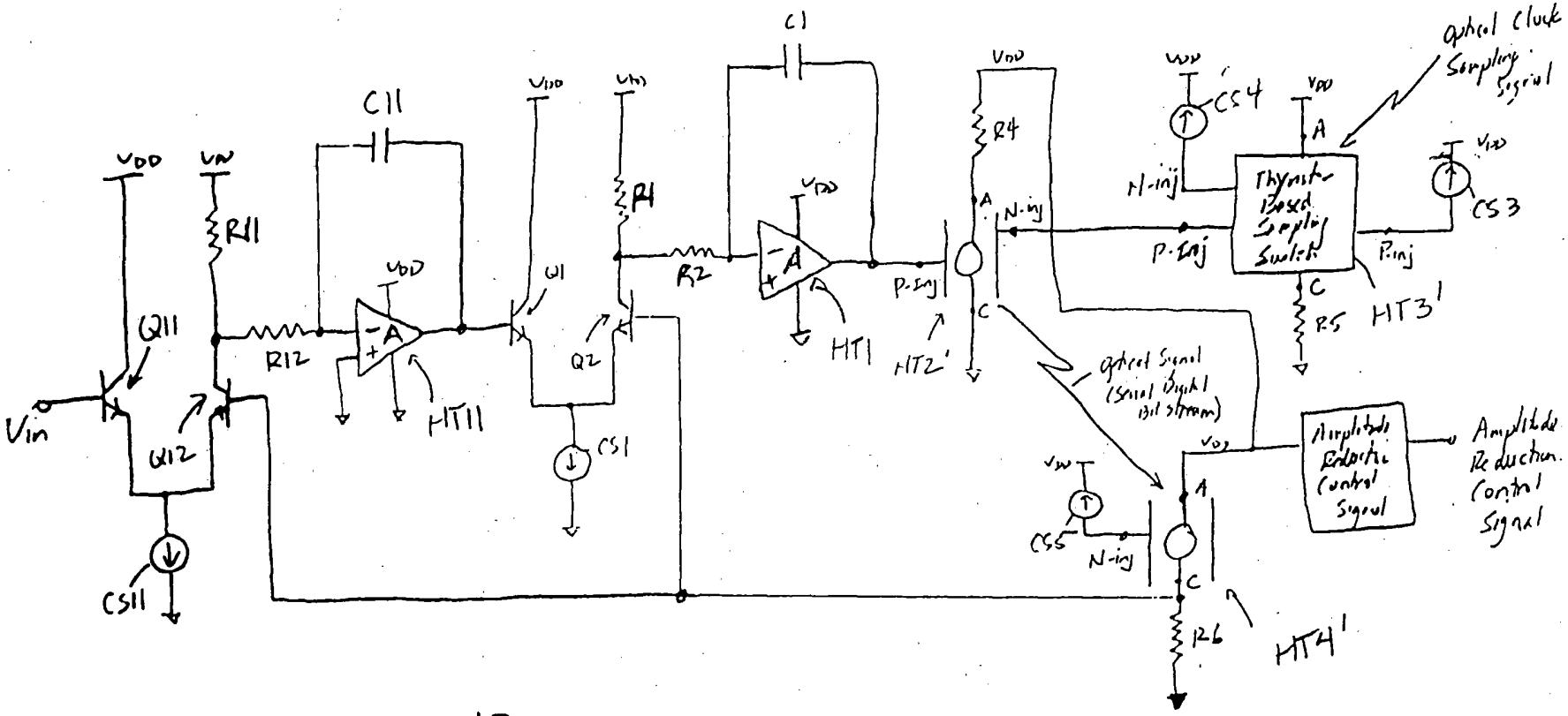

C1
C11
VDD
VW
R11
R12
Q11
Q12
CS11
Vin
HT11
Q1
Q2
R1
R2
CS1
HT1
P-inj
HT2'
R4
N-inj
CS4
optical Clock Sampling signal
Thyristor Based Sampling Switch
P-inj
CS3
R5
HT3'
optical Signal (Serial Digital bit stream)
Amplitude Reduction Control Signal
CS5
R6
HT4'

FIG. 4B2

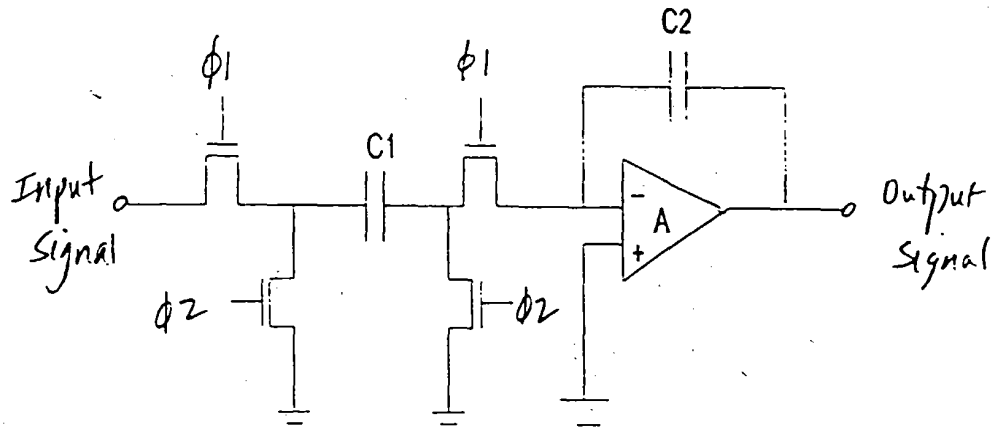


FIG. 4B3

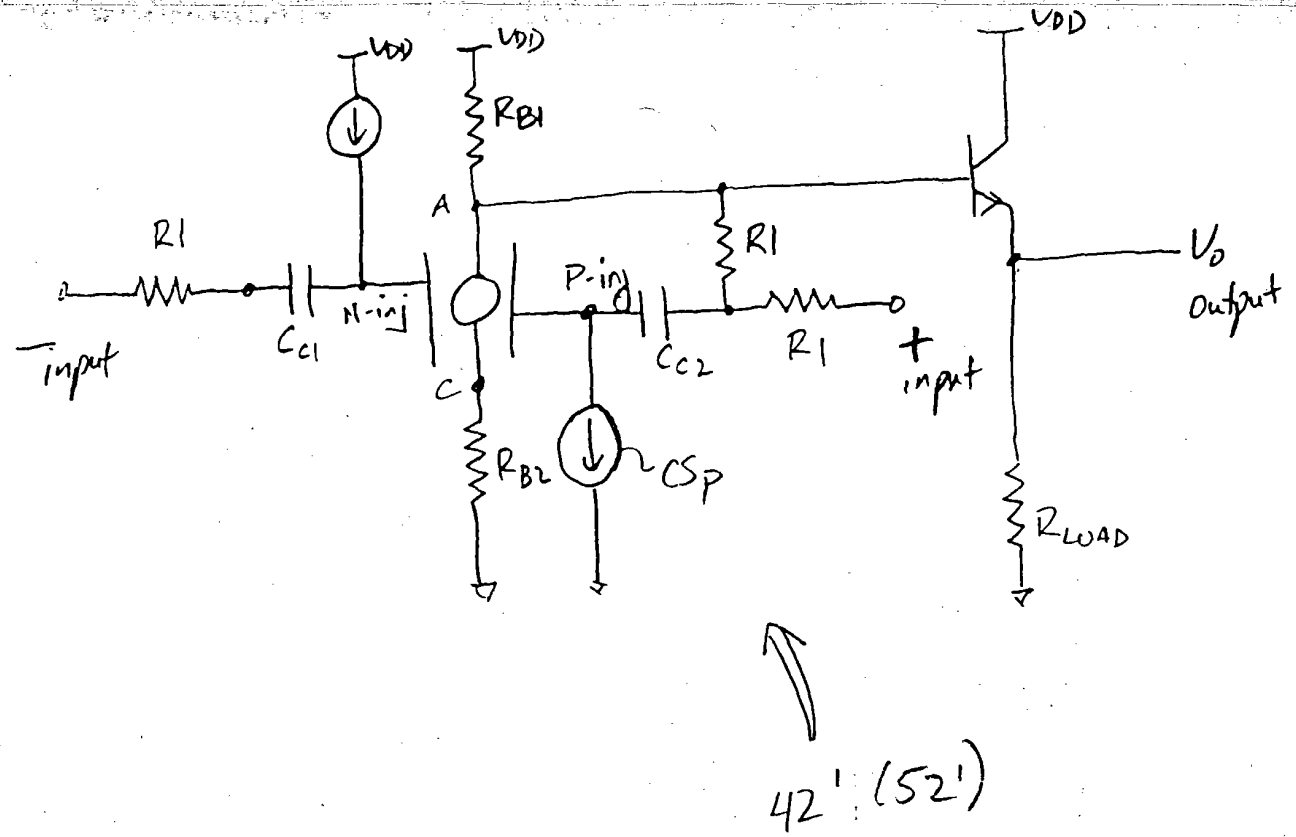


FIG. 4B4

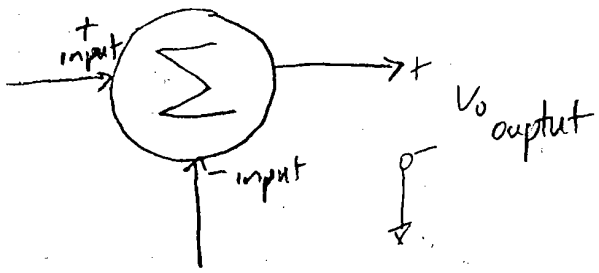


FIG. 4B5

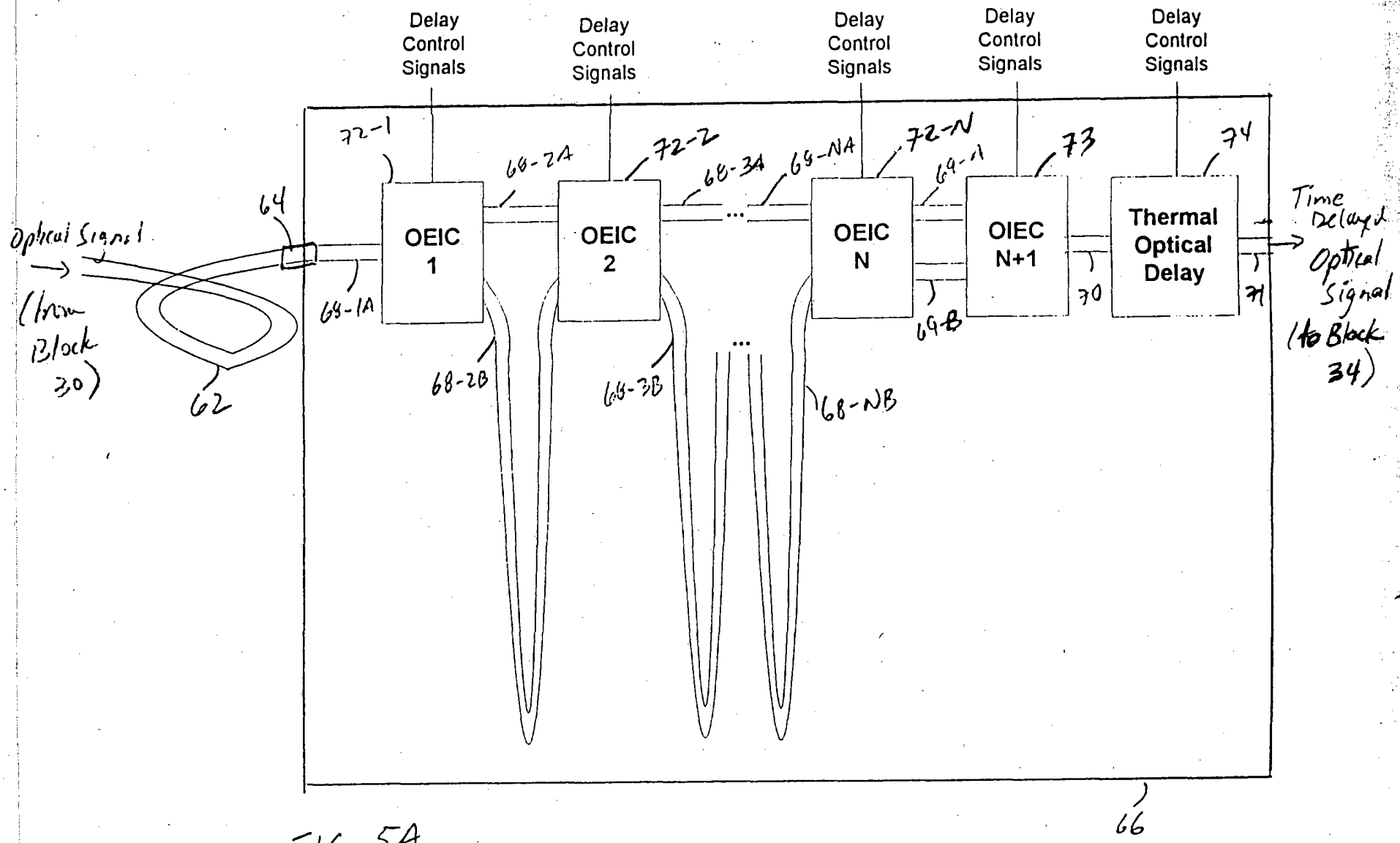

Delay Control Signals
Delay Control Signals
Delay Control Signals
Delay Control Signals
Delay Control Signals
72-1
72-2
72-N
73
74
64
Optical Signal
(from Block 30)
62
OEIC 1
OEIC 2
OEIC N
OIEC N+1
Thermal Optical Delay
68-1A
68-2A
68-3A
68-NA
69-1
69-B
70
71
68-2B
68-3B
68-NB
Time Delayed Optical Signal (to Block 34)
66

FIG. 5A

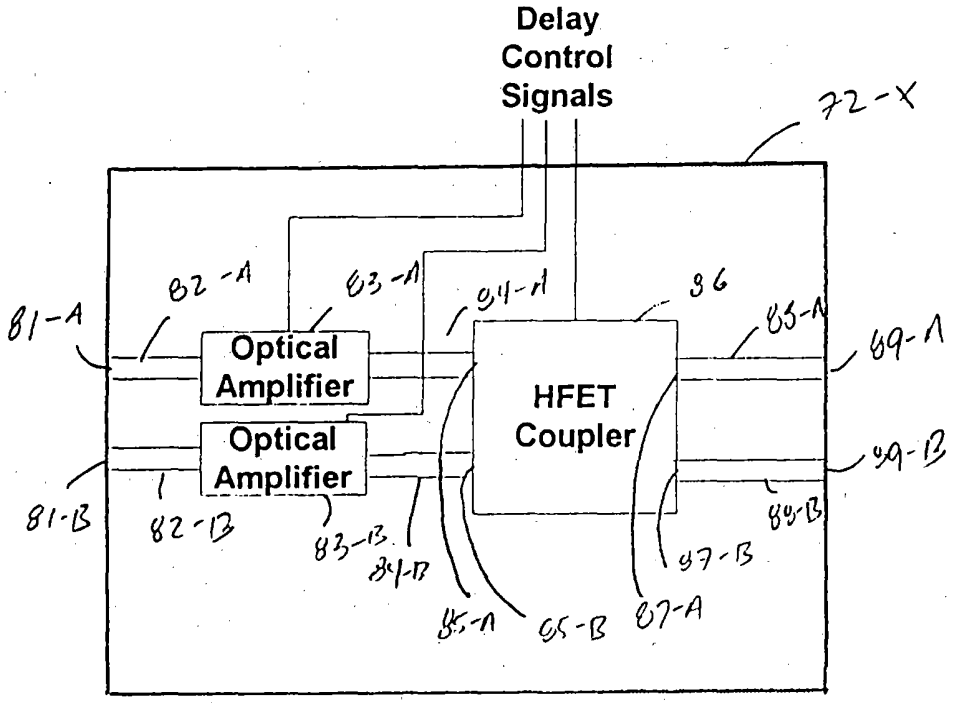
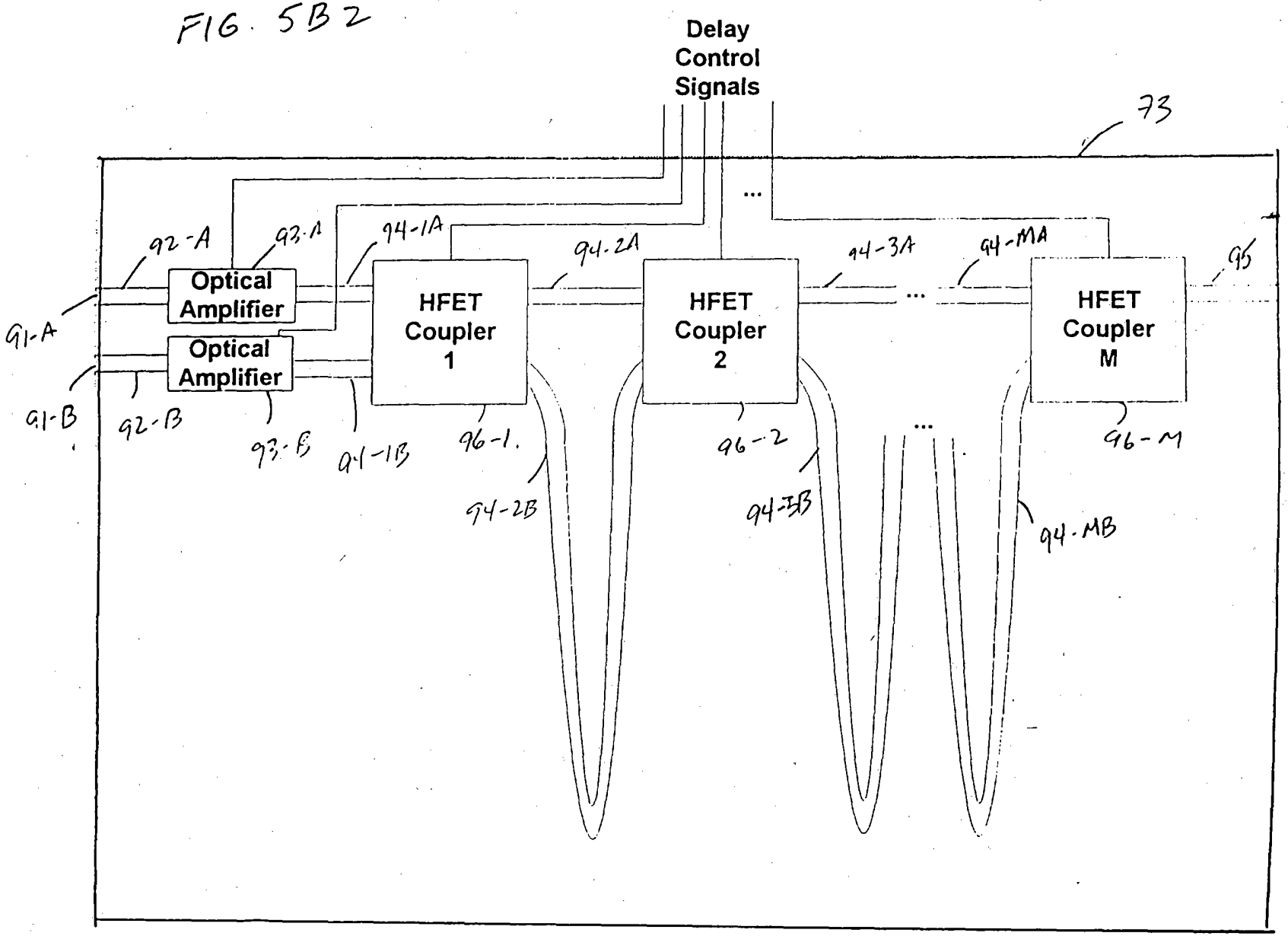

Delay
Control
Signals
72-X
81-A
82-A
83-A
84-A
86
85-A
89-A
Optical
Amplifier
HFET
Coupler
Optical
Amplifier
89-B
81-B
82-B
83-B
84-B
85-A
85-B
87-A
87-B
88-B

FIG. 5B1

FIG. 5B2


Delay Control Signals
73
Optical Amplifier
Optical Amplifier
HFET Coupler 1
HFET Coupler 2
HFET Coupler M
91-A
91-B
92-A
92-B
93-A
93-B
94-1A
94-1B
94-2A
94-2B
94-3A
94-MA
94-MB
95
96-1
96-2
96-M

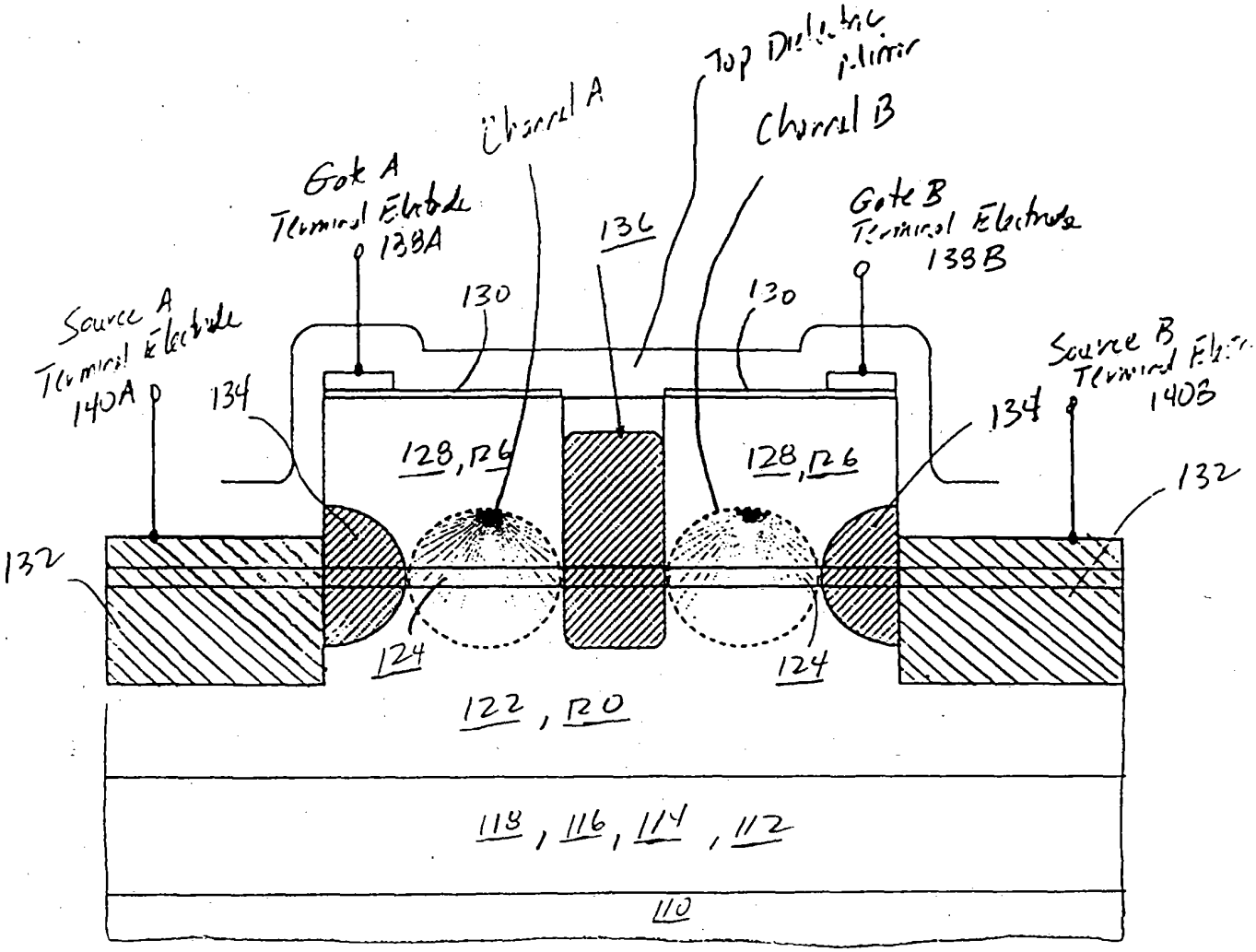

Top Dielectric Layer
Channel A
Channel B
Gate A Terminal Electrode 138A
Gate B Terminal Electrode 138B
136
130
130
Source A Terminal Electrode 140A
134
134
Source B Terminal Electrode 140B
128, 126
128, 126
132
132
124
124
122, 120
118, 116, 114, 112
110

FIG 5C1

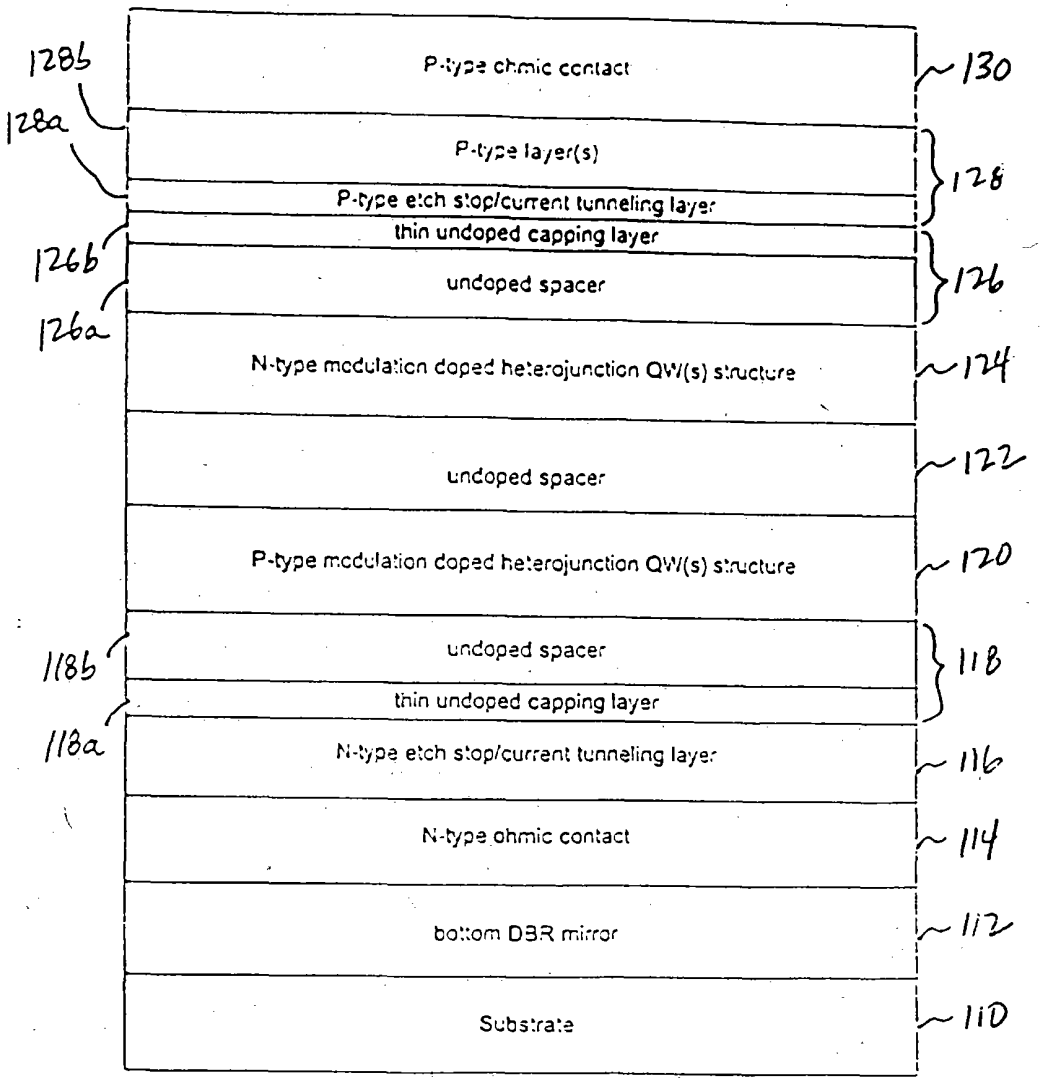

128b
128a
126b
126a
118b
118a
P-type ohmic contact
P-type layer(s)
P-type etch stop/current tunneling layer
thin undoped capping layer
undoped spacer
N-type modulation doped heterojunction QW(s) structure
undoped spacer
P-type modulation doped heterojunction QW(s) structure
undoped spacer
thin undoped capping layer
N-type etch stop/current tunneling layer
N-type ohmic contact
bottom DBR mirror
Substrate
130
128
126
124
122
120
118
116
114
112
110

FIG. 5C2

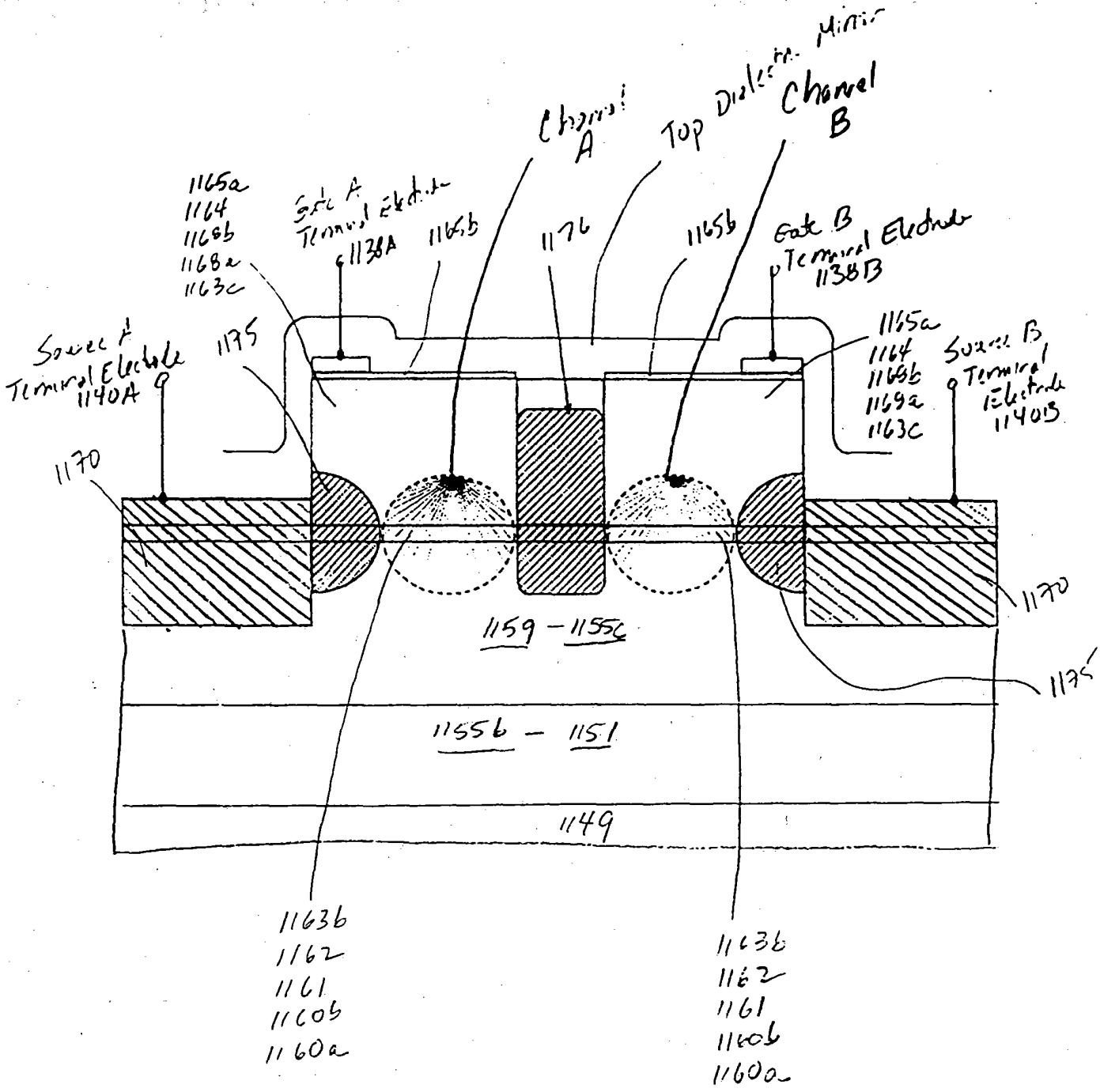

Channel A
Top Dielectric Mirror
Channel B
1165a
1164
1166b
1168a
1163c
Gate A Terminal Electrode
1138A
1166b
1176
1165b
Gate B Terminal Electrode
1138B
Source A Terminal Electrode
1140A
1175
1165a
1164
1166b
1169a
1163c
Source B Terminal Electrode
1140B
1170
1170
1159 – 1155c
1175
1155b – 1151
1149
1163b
1162
1161
1160b
1160a
1163b
1162
1161
1160b
1160a

FIG. 5D1

Layer Material	Layer Doping Type	Typical Doping Concentration (atoms/cm^{-3})	Typical Layer Thickness (A)	Layer #	
InGaAs	p+	1E20	25	1165b	130
GaAs	p+	1E20	75	1165a	
GaAs	p	1-5E17	300	1164	128
AlAs	p+	3.5E18	>20 , <300	1168b	
GaAs	und	und	>6, <20	1168a	126
Al.15Ga.85As	und	und	200 - 300	1163c	
Al.15Ga.85As	n+	3.5E18	80	1163b	124
Al.15Ga.85As	und	und	20-30	1163a	
GaAs	und	und	15	1162	
In.15Ga.85AsN	und	und	60	1161	
GaAs (x3)	und	und	100	1160b	
GaAs	und	und	100 - 250	1160a	
Al.15Ga.85As	und	und	5000	1159	122
GaAs	und	und	250 - 500	1167	
GaAs	und	und	100	1158	120
In.15Ga.85AsN (x3)	und	und	60	1157	
GaAs	und	und	15	1156	
Al.15Ga.85As	und	und	30	1155d	
Al.15Ga.85As	P+	3.5E18	80	1155c	
Al.15Ga.85As	und	und	200-300	1155b	118
GaAs	und	und	>6 , <20	1166b	
AlAs	N+	3.5E18	>30 , <200	1166a	116
GaAs	N+	3.5E18	1000 - 2000	1153	114
AlAs	und	und	1701	1151	112
GaAs (x7)	und	und	696	1152	
AlAs	und	und	1701	1151	
GaAs Substrate		SI		1149	110

128b
128a
126b
126a
118b
118a

FIG 5D2

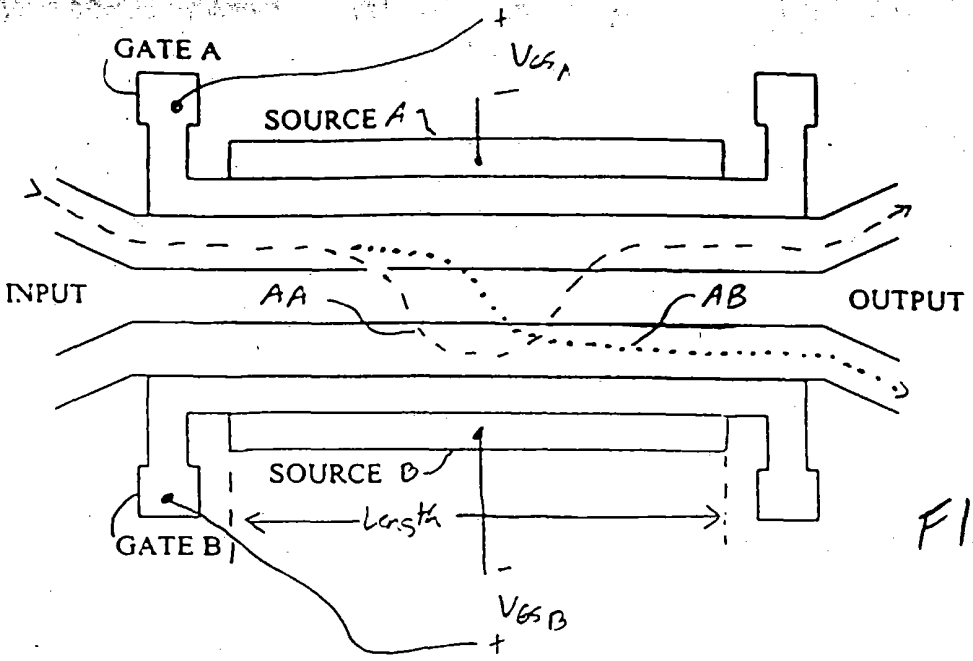


FIG. 5E1

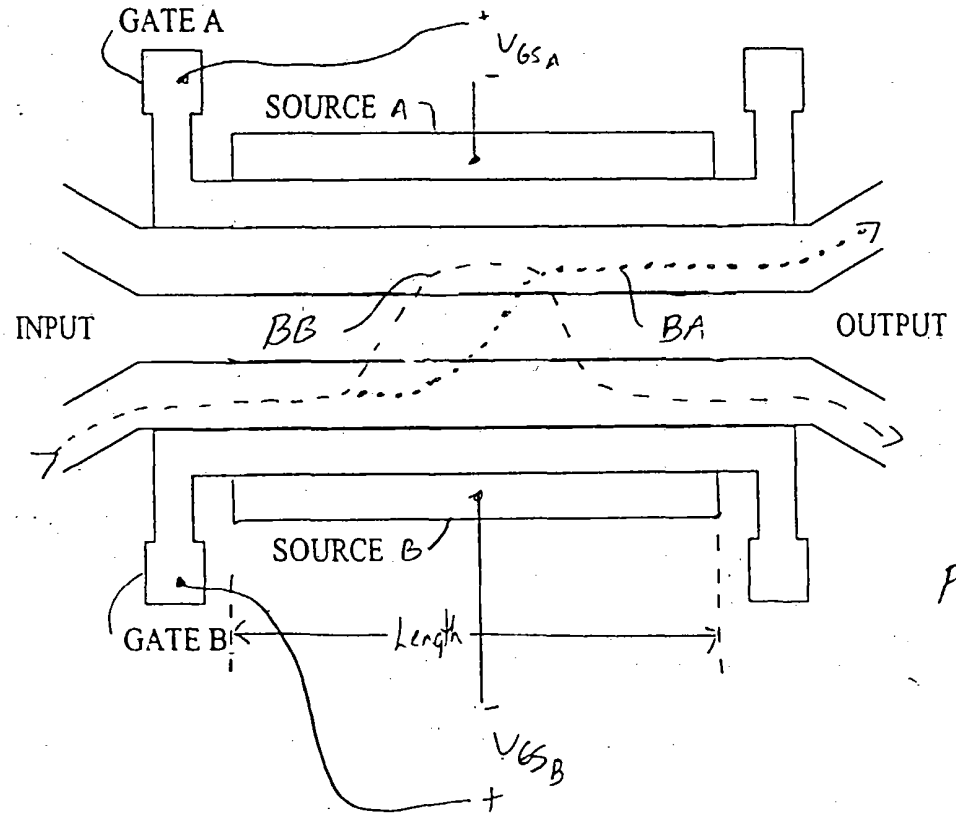


FIG. 5E2

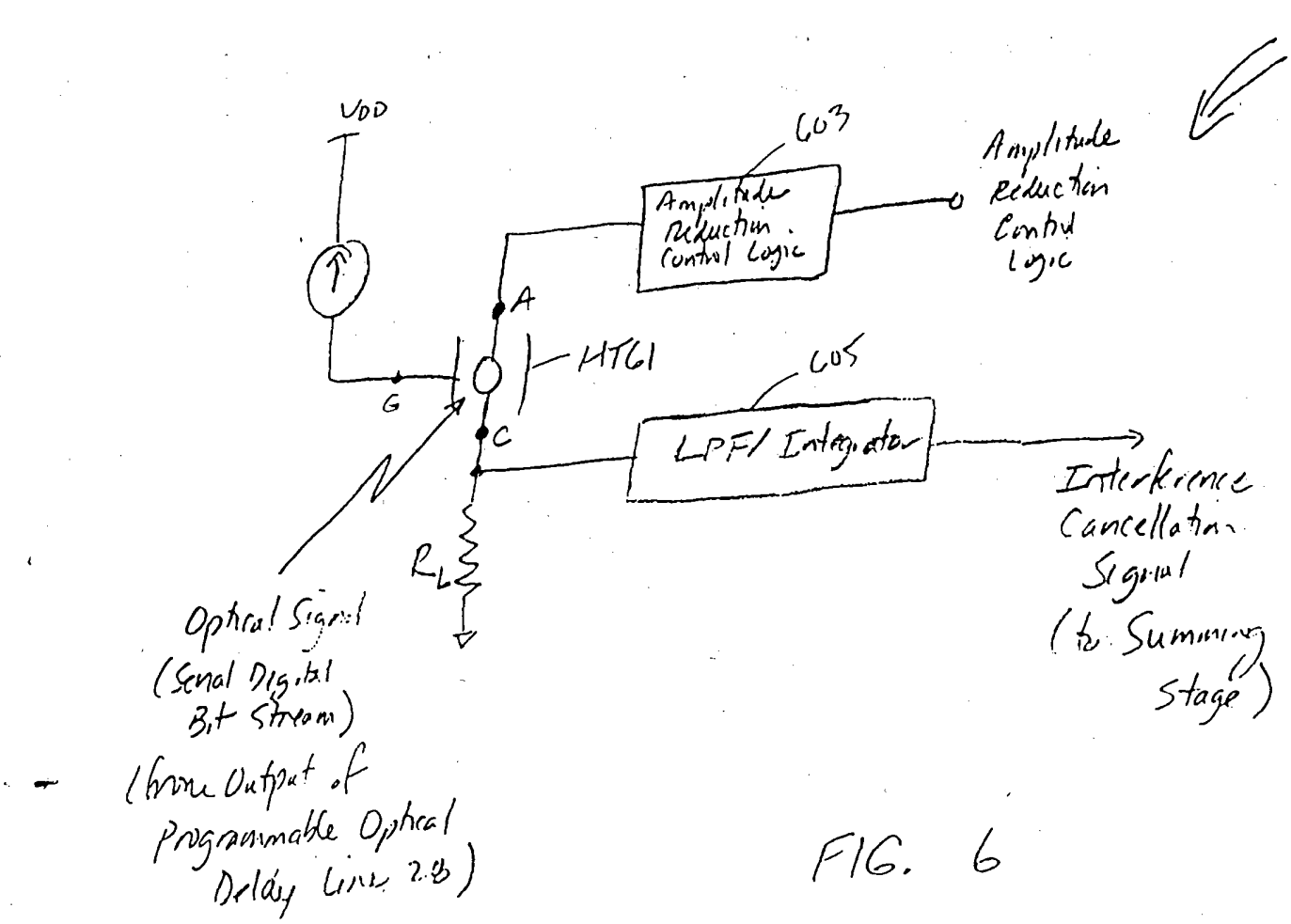

341
VDD
603
Amplitude Reduction Control Logic
Amplitude Reduction Control Logic
A
HTG1
605
G
C
LPF/ Integrator
Interference Cancellation Signal (to Summing Stage)
R_L
Optical Signal (Serial Digital Bit Stream)
(from Output of Programmable Optical Delay Line 28)

FIG. 6

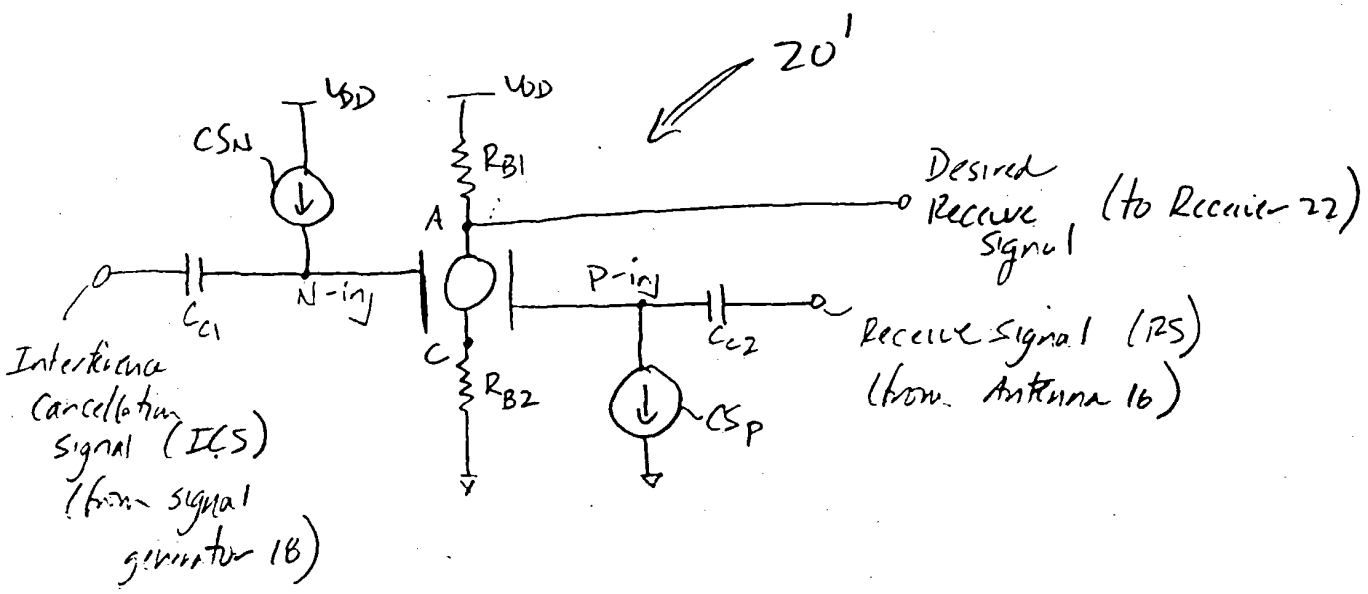

20'
V_{DD}
V_{DD}
CS_N
R_{B1}
A
Desired Receive Signal (to Receiver 22)
N-inj
P-inj
C_{C1}
C_{C2}
C
R_{B2}
CS_P
Receive Signal (RS) (from Antenna 16)
Interference Cancellation Signal (ICS) (from signal generator 18)

FIG. 7A

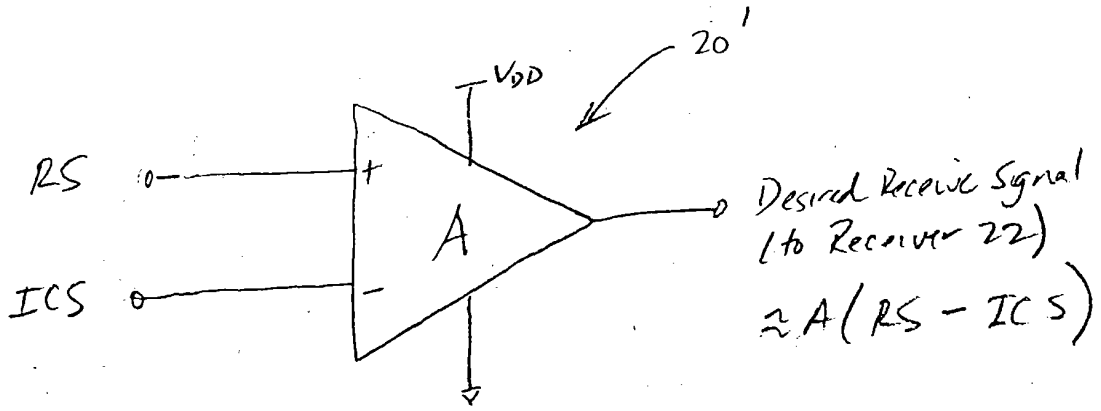

20'
V_{DD}
RS
ICS
+
−
A
Desired Receive Signal (to Receiver 22)
$\simeq A(RS - ICS)$

FIG. 7B